REMARKS

Applicant thanks the Examiner for the careful review of this application. Claims 1 and 6 were amended to clarify aspects of the present invention. No new matter was added. Claims 1-9 remain pending in this application.

REJECTIONS UNDER 35 U.S.C. § 112, FIRST PARAGRAPH

Claims 1-8 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement. Applicant respectfully traverses theses rejection. However, the affected claims have been amended and therefore these rejections are now moot.

APPLICANT'S CLAIMED EMBODIMENTS

Applicant's specification discloses that a time difference TM is adjustable. TM defines the time difference between CLK1/CLK2 and CLK2/CLK3. TM for the two regions is always equal but it is still adjustable such that a valid data region can accurately be maintained as the eye opening changes. That is, the whole distribution between CLK1 and CLK3 can be moved left or right and the value of TM can additionally be increased or decreased. This is fully described via Applicant's Fig. 3A and in the specification:

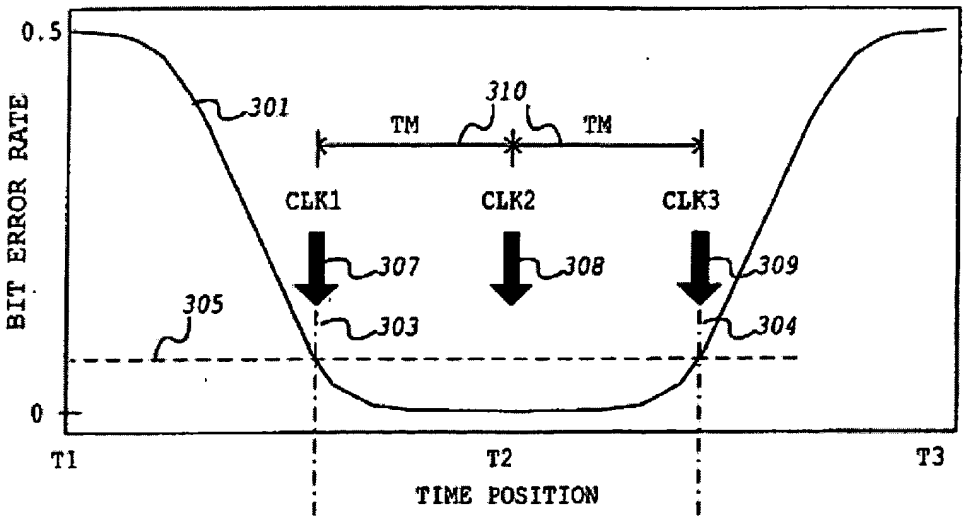


FIG. 3a

[0026] In the present invention, 'CLK2' **308** is controlled by a phase control signal that is determined from the difference of the bit-error-rate measured at 'CLK1' **307** and the one measured at 'CLK3' **309**. 'CLK1' **307** and 'CLK3' **309** are advanced and delayed from 'CLK2' **308** by the time difference of 'TM' **310**, respectively. The time difference 'TM' **310** is controlled by another phase control signal that is determined from the summation of the two bit-error-rate. If bit-error-rate at 'CLK1' **307** is greater than the one at 'CLK3' **309**, it means that the overall sampling phase leads the eye opening. Therefore, the phase of 'CLK2' **308** is delayed until the two bit-error-rate becomes equal. On the contrary, if the bit-error-rate at 'CLK1' **307** is smaller, the phase of 'CLK2' **308** is advanced. If the sum of the two bit-error-rate exceeds a predetermined value, 'TM' **310** is decreased to shrink the sampling window to the eye opening. If the sum is less than predetermined value, 'TM' **310** is increased.

-Applicant's specification, paragraph 26

Applicant has amended independent claims 1 and 6 to reflect the above-described embodiment such that a time distance between a first-occurring clock of the plurality of clocks and a last-occurring clock of the plurality of clocks is

automatically adjustable. Withdrawal of the rejections of claims 1-8 is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 102(b)

Claims 1, 4 and 6 were rejected under 35 U.S.C. § 102(e) as being anticipated by Bergmann (U.S. Patent No. 4,821,297). Claim 9 was rejected under 35 U.S.C. § 102(e) as being anticipated by Hogge (U.S. Patent No. 4,218,771). Applicant respectfully traverses for the following reasons.

Bergman apparently discloses a digital clock recovery scheme. Included is reference clock used to provide a plurality of N signals with different clock phases. The incoming data stream is sampled and clocked with the reference clock to generate a plurality of M samples for each data bit. The logic values of the M samples are then analyzed to determine the relationship between the current clock phase and the data bit transition. If all samples agree, the clock phase is perhaps aligned with the data. If the clock phase is either leading or lagging the data, various samples will disagree. In the latter situation, the clock phase is adjusted until all samples agree, the particular clock which provides this state thus being defined as the recovered clock signal.

Hogge apparently discloses an automatic clock positioning circuit for positioning a clock pulse for a digital data stream that resembles an eye pattern when seen on an oscilloscope in response to digital data when the sweep is equal to the baud, bit or clock rate. Included in the circuit is a timing source for providing a stream of clock pulses and a controllable phase shift means electrically connected to said timing source and in response to an error signal will either advance, delay or maintain the phase of said stream of clock pulses. Also

included is a pseudo-error indicator means for providing an upper, lower, early and late boundary condition within the center of the eye pattern of the digital data stream and providing a first pseudo-error signal for each violation of the upper or lower boundary condition by the eye pattern at the early boundary condition and a second pseudo-error signal for each violation of the upper and lower boundary condition at the late boundary of the eye pattern, means for integrating the first and second error signals, means for comparing the integrated first error signal with the integrated second pseudo-error signal providing an error correcting signal; and means for controlling the controllable phase shift means with the error connecting signal.

Aspects of the claimed embodiments are directed to methods and systems for data recovery for a digital stream of input data such that a plurality of sampling clocks are employed to maintain optimal placement of a valid data region within an eye opening that results from a superposition of multiple data transitions. The entire width of the valid data region can be adjusted smaller or larger and moved to the left or right to maintain optimal placement. For example, the valid data region may need to only be adjusted on the left side due to an asymmetrical jitter distribution. The valid data region can be expanded and also moved to match that asymmetrical jitter distribution. Advantageously, the claimed embodiments allow for adjustment of the valid data region, as defined by a leading and trailing clock, as the shape of the jitter distribution changes as well as mere shifts of the center of the distribution to the left or right. This behavior is fully described in Applicant's specification:

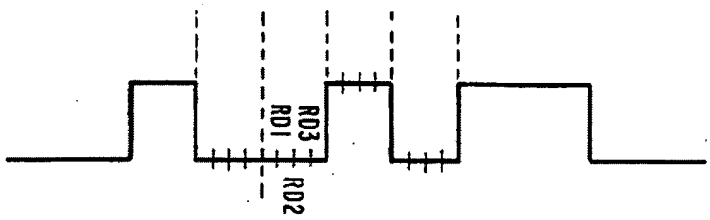
[0026] In the present invention, 'CLK2' 308 is controlled by a phase control signal that is determined from the difference of the bit-error-rate measured at 'CLK1' 307 and the one measured at 'CLK3' 309. 'CLK1' 307 and 'CLK3' 309 are advanced and delayed from 'CLK2' 308 by the time difference of 'TM' 310, respectively. The time difference 'TM' 310 is controlled by another phase control signal that is determined from the summation of the two bit-error-rate. If bit-error-rate at 'CLK1' 307 is greater than the one at 'CLK3' 309, it means that the overall sampling phase leads the eye opening. Therefore, the phase of 'CLK2' 308 is delayed until the two bit-error-rate becomes equal. On the contrary, if the bit-error-rate at 'CLK1' 307 is smaller, the phase of 'CLK2' 308 is advanced. If the sum of the two bit-error-rate exceeds a predetermined value, 'TM' 310 is decreased to shrink the sampling window to the eye opening. If the sum is less than predetermined value, 'TM' 310 is increased.

-Applicant's specification, paragraph 26

In marked contrast, both Bergman and Hogge disclose methods of maintaining an optimal clock position in an eye of a jitter distribution via fixed valid data regions. That is, the leading and trailing sample clocks that define the valid data region are pre-defined at a set and equal distance on either side of the data clock. If the valid data region, or conversely the eye opening moves, to either side then both Bergman and Hogge will make an adjustment of the valid data region as a whole in the appropriate direction to correct the phase imbalance. Disadvantageously, both Bergman and Hogge are simply not capable of adjusting the size of their valid data region.

To further illustrate, Applicant respectfully draws the attention of the Examiner to Bergmann's Fig. 2 and column 3, line 63 to column 4, line 17 that are reproduced here:

FIG. 2



Referring to FIG. 2, a timing diagram is shown of incoming data. The clock signal is represented by the vertical lines. The locations of RD1, RD2, and RD3 for each data bit are indicated by their respective numerals in FIG. 2. For this particular example, RD1 may represent the 10% interval of the data bit, RD2 the 50% interval, and RD3 the 90% interval. Other interval values for RD1 and RD3 may be used, for example, 25% and 75%, respectively. In accordance with the teachings of the present invention, however, the middle sample value must be chosen at or near the 50% interval since this position of the data bit will most likely represent the correct data bit value, regardless of the initial misalignment of the clock. Therefore, RD2 is utilized as the retimed data output of recovery arrangement 10. For the particular situation illustrated in FIG. 2, data samples RD1, RD2 and RD3 will always be identical in value, since the phase of the clock is correctly synchronized with the data stream. That is, the RD1-RD2-RD3 inputs to decision circuit 18 will either be "1-1-1" or "0-0-0." Provided with this input, decision circuit 20 will transmit a "no change" output signal to phase selector 22.

- Bergmann

Bogge's out of phase alignment system is dependent on the spacing of the "RD" marks in the timing diagram. Alignment is achieved when a specific pattern is detected. The "RD" marks can perhaps be adjusted but then that would perhaps require the pattern to be changed accordingly to properly detect alignment. The spacing of the RD marks are not automatically changed in response to a change in the width of the timing pulses.

Hogge also discloses a similar type of system that is dependent on the eye pattern moving out of a specified and fixed window such as that described by Hogge's Fig. 2 and at column 3, lines 36-48:

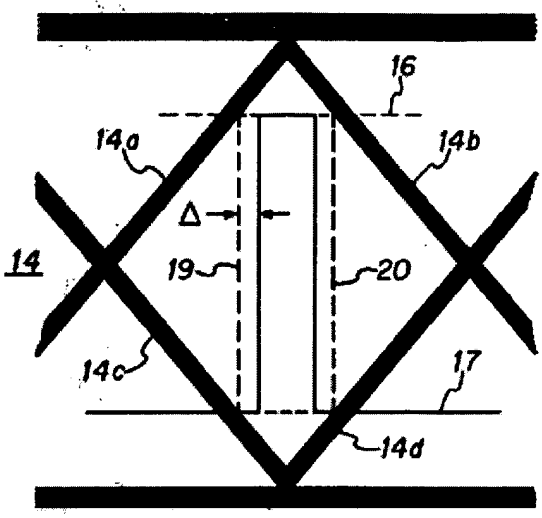


FIG. 2

There is established an upper boundary condition 16 and a lower boundary condition 17 in the eye pattern. The timing pulses τ_2 as shown by waveform 7 in FIG. 1 establish the early boundary condition 19 while the delayed boundary condition 20 is established by the delayed timing pulses τ_1 of waveform 11 of FIG. 1. Under ideal conditions, the clock or timing pulses associated with each data bit will occur in the center of the eye pattern. However, when a side 14*a*, 14*b*, 14*c* or 14*d* of the eye pattern crosses the boundary conditions established by the upper boundary 16, the lower boundary 17, the early clock pulse τ_2 at 19 or the late clock pulse τ_1 at 20, then a pseudo-error occurs.

- Hogge

Hogge specifies that the eye pattern is out of alignment when the upper boundaries 16 and 17 intersect with eye pattern boundaries 14a, 14b, 14c or 14d. No disclosure is made of adjusting these various boundaries in response to a change in the shape of the eye pattern.

Regarding claim 9, claim 9 specifies that "said sampling points are arranged by a predetermined order and adjustable time difference". Again, Hogge does not disclose an adjustable time difference.

Claim 4 depends directly from independent claim 1 and is allowable at least for the reasons set forth for that independent claim. Withdrawal of the rejections of claims 1, 4, 6 and 9 is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 2-3 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bergmann in view of Hogge.

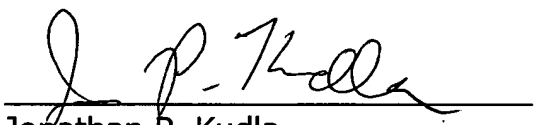
Bergmann and Hogge were previously summarized. Since claims 2-3 and 7 depend from independent claims 1 and 6, Applicant respectfully submits that these claims are also allowable at least for the reasons put forth in the previous section. Withdrawal of the rejections of claims 2-3 and 7 are respectfully requested.

CONCLUSION

Applicant believes that all pending claims are allowable and a Notice of Allowance is respectfully requested. The amendment was made to expedite the prosecution of this application. Applicant respectfully traverses the rejections of the amended claims and reserves the right to re-introduce them and claims of an equivalent scope in a continuation application.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel at the number set out below.

Respectfully submitted,
PERKINS COIE LLP



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